T-61.123 Computer Architecture

Tik-61.123 Computer Architecture
Lecture 1 : Introduction

Course Administration

- Instructor: Lic. Tech Mikko Huttunen (mikko.i.huttunen@nokia.com)
- Assistant: MSc.Mika Rättö (tark@hut.fi)
- Assignment: SPIM simulator...
- Materials: Delivered via Otapaino
- Newsgroup: opinnot.tik.tark
- Text: *Computer Organization and Design: The Hardware/Software Interface,* ***Second Edition***, Patterson and Hennessy
  - Q: Need 2nd Edition?
    yes! >> 50% text changed, all exersizes changed all examples modernized, new sections, ...

Course Adminstration

- Course assistant's reception time is 8.15-9.15 AM at thursdays (27.9-18.10)
- Assistant's reception place is the library of laboratory of information technology (B322)
- The assignment work is *personal* (max. grade 3 or 5)
- Assistant advises in problems
- Assistant can be contacted with otax, at the reception or e-mail (preferred)
- Assignment work deadline is 19.10 4.00 PM
- The work will be returned to course box (in laboratory of information science)

Course adminstration

° **If the assignment work is not returned in time (before the deadline):**

* Grade is grade-1
* The assignment work will be checked in may 2002 !!!!

Course adminstration

° **Registration:*wwwTopi!***

° ***Grading:***

assignment work grade * 1/3

\+ exam grade * 2/3

= course grade

What is "Computer Architecture"

Computer Architecture =

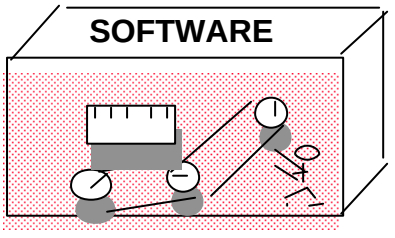
Instruction Set Architecture +

Machine Organization

Instruction Set Architecture (subset of Computer Arch.)

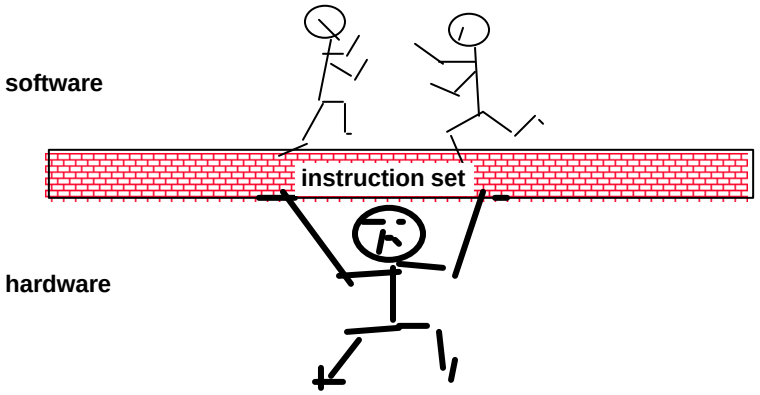
... the attributes of a [computing] system as seen by the programmer, *i.e.* the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls the logic design, and the physical implementation.

– Amdahl, Blaaw, and Brooks, 1964



- **Organization of Programmable Storage**
- **Data Types & Data Structures: Encodings & Representations**
- **Instruction Set**
- **Instruction Formats**
- **Modes of Addressing and Accessing Data Items and Instructions**
- **Exceptional Conditions**

The Instruction Set: a Critical Interface



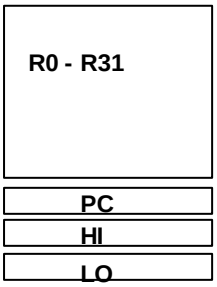
Example ISAs (Instruction Set Architectures)

° Digital Alpha	(v1, v3)	1992-97
° HP PA-RISC	(v1.1, v2.0)	1986-96
° Sun Sparc	(v8, v9)	1987-95
° SGI MIPS	(MIPS I, II, III, IV, V)	1986-96
° Intel	(8086,80286,80386, 80486,Pentium, MMX, ...)	1978-96

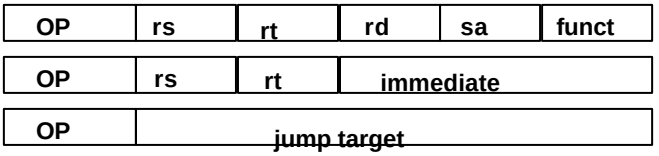
MIPS R3000 Instruction Set Architecture (Summary)

° **Instruction Categories**
- Load/Store
- Computational
- Jump and Branch
- Floating Point
  - coprocessor
- Memory Management
- Special

Registers



3 Instruction Formats: all 32 bits wide



Q: How many already familiar with MIPS ISA?

Organization

° **Capabilities & Performance Characteristics of Principal Functional Units**
- (e.g., Registers, ALU, Shifters, Logic Units, ...)

° **Ways in which these components are interconnected**

° **Information flows between components**

° **Logic and means by which such information flow is controlled.**

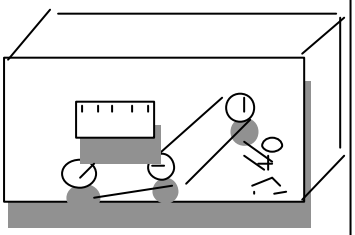
° **Choreography of FUs to realize the ISA**

° **Register Transfer Level (RTL) Description**

Logic Designer's View

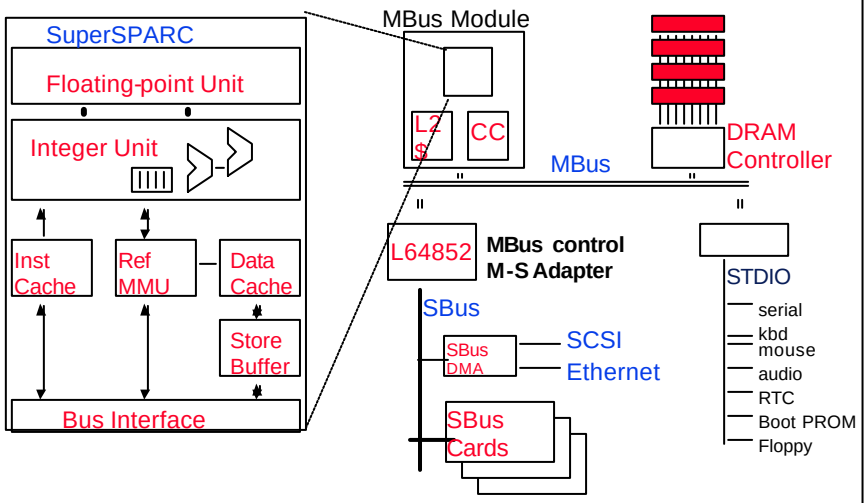
ISA Level

FUs & Interconnect

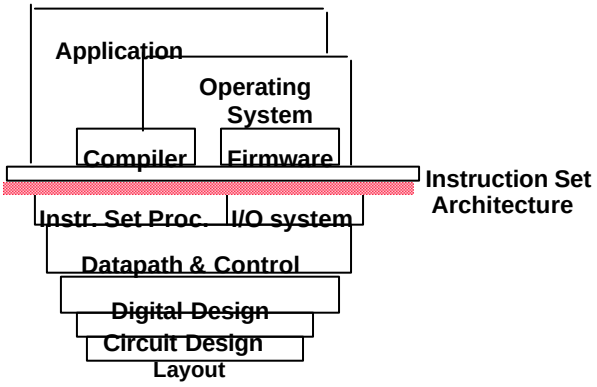


Example Organization

° TI SuperSPARC^{tm} TMS390Z50 in Sun SPARCstation20



What is "Computer Architecture"?

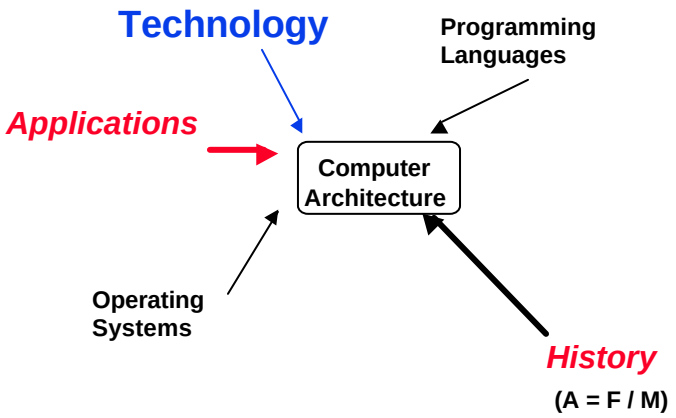


° Coordination of many *levels of abstraction*

° Under a rapidly changing set of forces

° Design, Measurement, *and* Evaluation

Forces on Computer Architecture

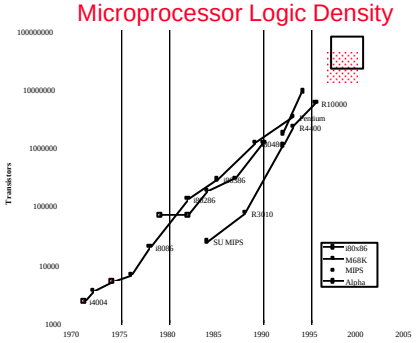


Technology

DRAM chip capacity

DRAM	
Year	Size
1980	64 Kb
1983	256 Kb
1986	1 Mb
1989	4 Mb
1992	16 Mb
1996	64 Mb
1999	256 Mb
2002	1 Gb

Microprocessor Logic Density



- In ~1985 the single-chip processor (32-bit) and the single-board computer emerged
  - => workstations, personal computers, multiprocessors have been riding this wave since
- In the 2002+ timeframe, these may well look like mainframes compared single-chip computer (maybe 2 chips)

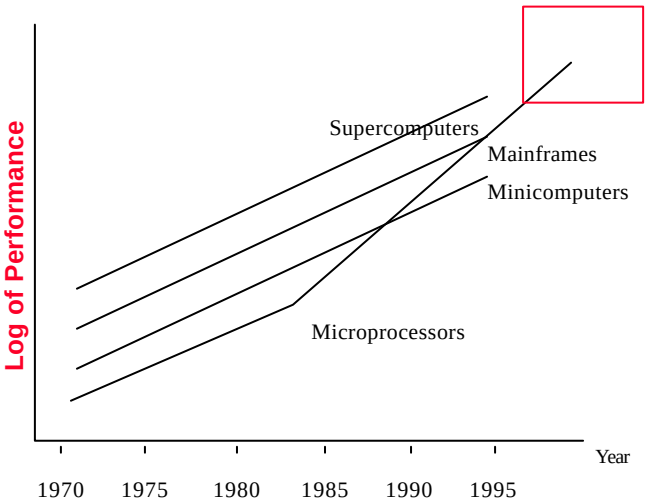
Technology => dramatic change

° **Processor**
- **logic capacity: about 30% per year**
- **clock rate: about 20% per year**

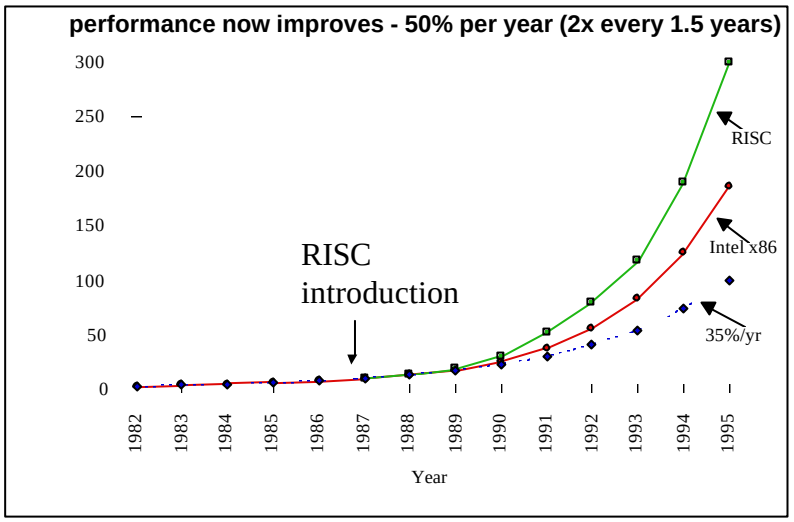
° **Memory**
- **DRAM capacity: about 60% per year (4x every 3 years)**
- **Memory speed: about 10% per year**
- **Cost per bit: improves about 25% per year**

° **Disk**
- **capacity: about 60% per year**

Performance Trends



Processor Performance (SPEC)

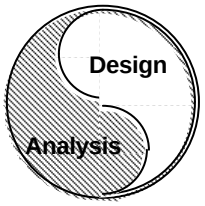


Did RISC win the technology battle and lose the market war?

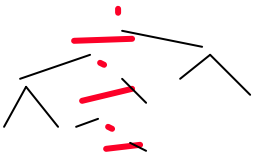
Applications and Languages

- CAD, CAM, CAE, . . .
- Lotus, DOS, . . .
- Multimedia, . . .
- The Web, . . .
- JAVA, . . .
- ???

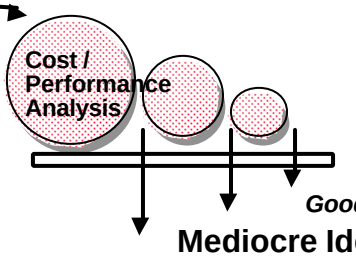
Measurement and Evaluation



Architecture is an iterative process
-- searching the space of possible designs
-- at all levels of computer systems



Creativity

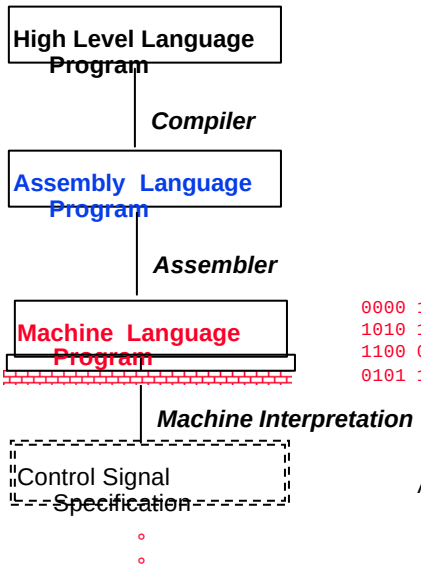


Good Ideas

Mediocre Ideas

Bad Ideas

Levels of Representation (61C Review)



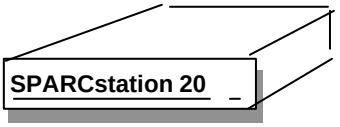

```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw $15, 0($2)
lw $16, 4($2)
sw $16, 0($2)
sw $15, 4($2)
```

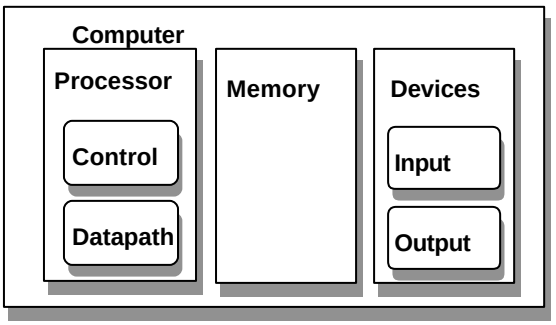
```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

ALUOP[0:3] <= InstReg[9:11] & MASK

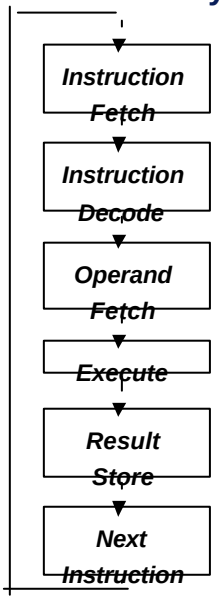
Levels of Organization



Workstation Design Target:
25% of cost on Processor
25% of cost on Memory
(minimum memory size)
Rest on I/O devices,
power supplies, box



Execution Cycle



Obtain instruction from program storage

Determine required actions and instruction size

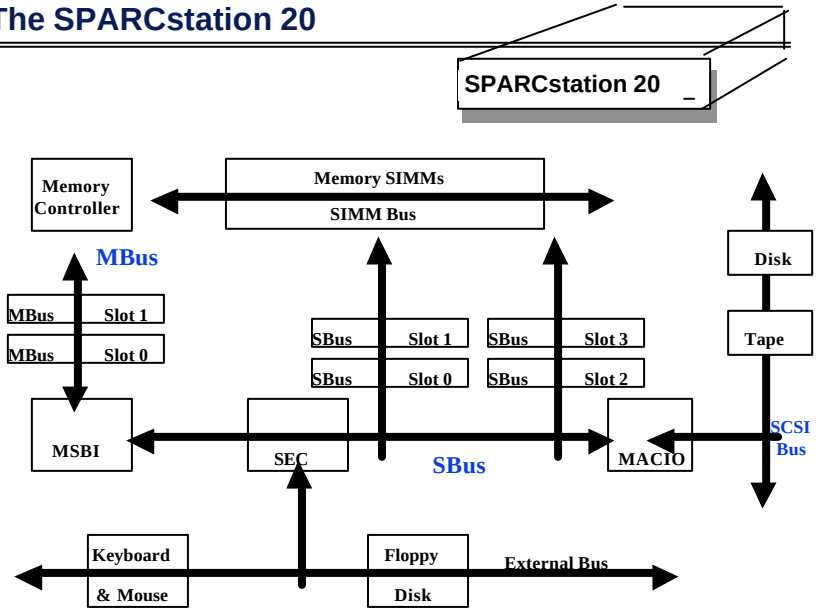
Locate and obtain operand data

Compute result value or status

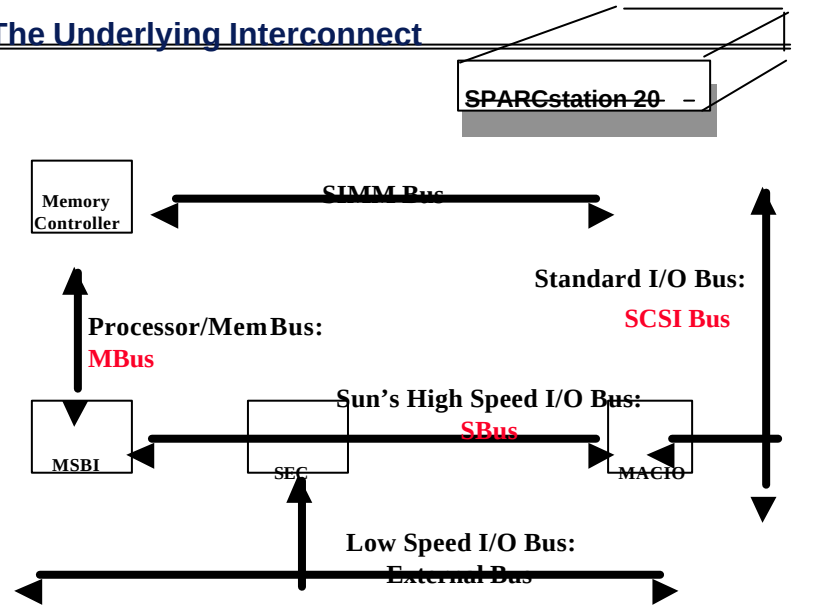
Deposit results in storage for later use

Determine successor instruction

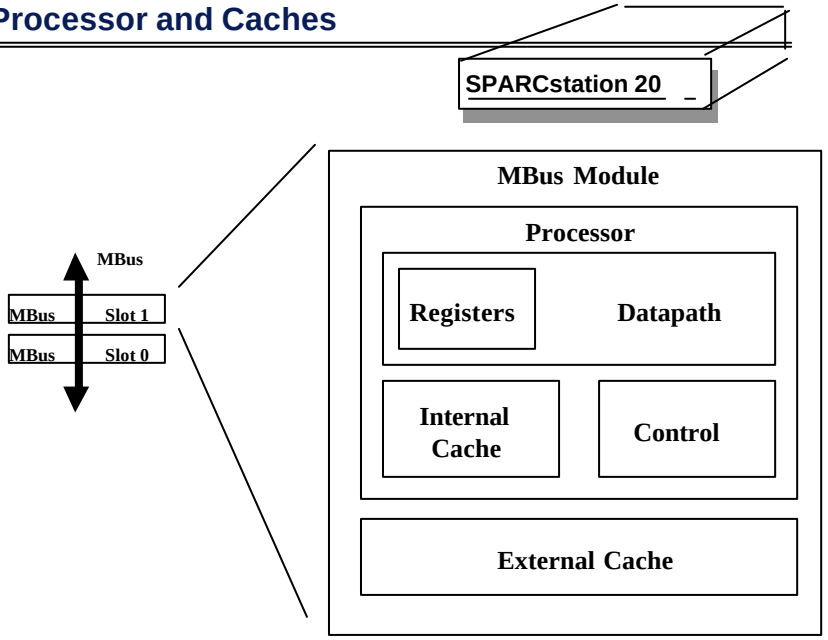
The SPARCstation 20



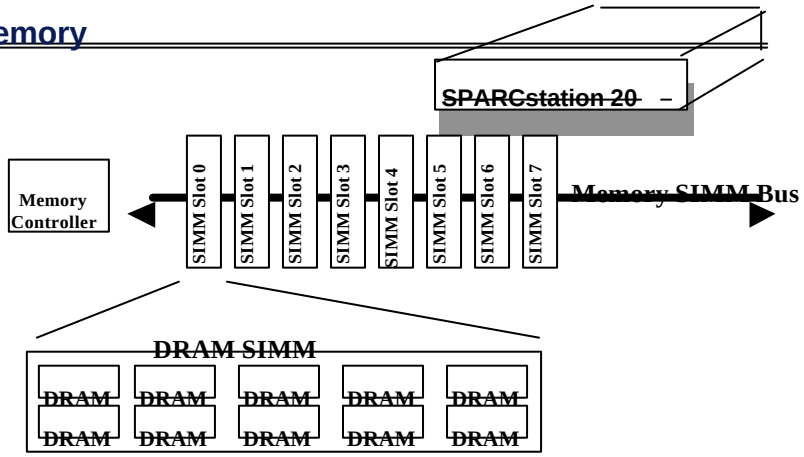
The Underlying Interconnect



Processor and Caches

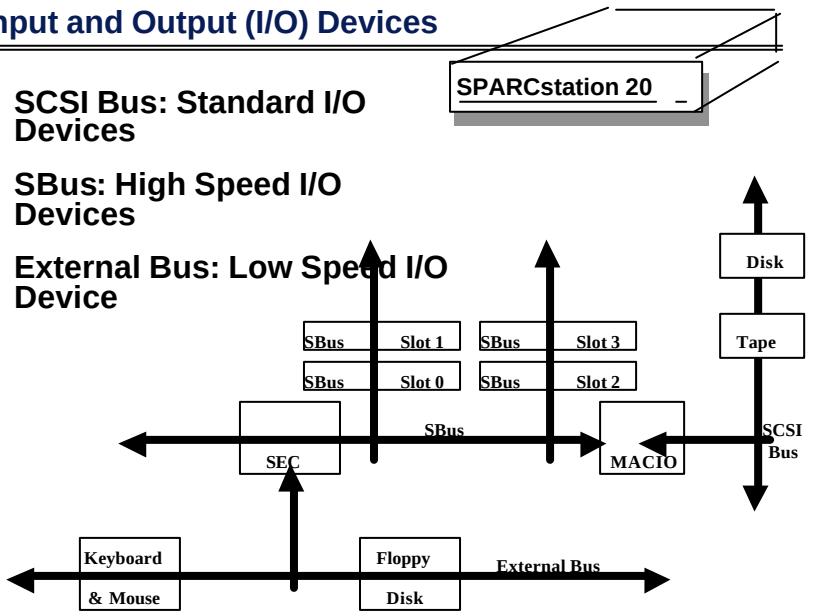


Memory

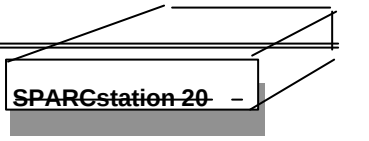


Input and Output (I/O) Devices

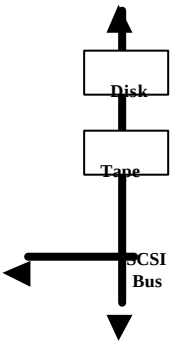
- SCSI Bus: Standard I/O Devices
- SBus: High Speed I/O Devices
- External Bus: Low Speed I/O Device



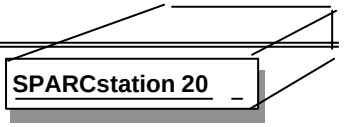
Standard I/O Devices



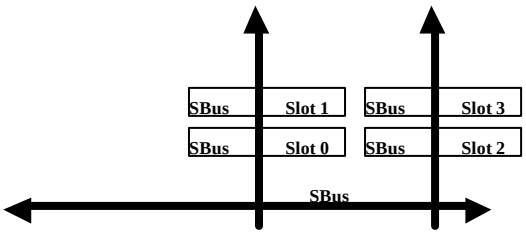
- SCSI = Small Computer Systems Interface
- A standard interface (IBM, Apple, HP, Sun ... etc.)
- Computers and I/O devices communicate with each other
- The hard disk is one I/O device resides on the SCSI Bus



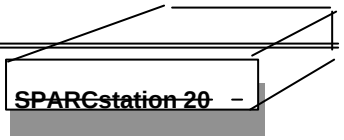
High Speed I/O Devices



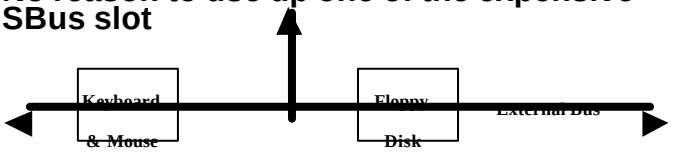
- SBus is SUN's own high speed I/O bus
- SS20 has four SBus slots where we can plug in I/O devices
- Example: graphics accelerator, video adaptor, ... etc.
- High speed and low speed are relative terms



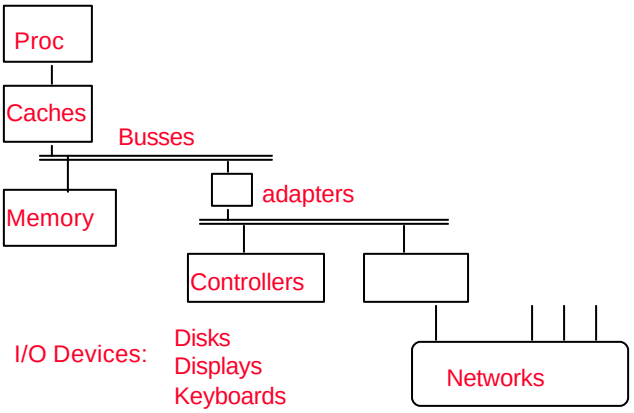
Slow Speed I/O Devices



- The are only four SBus slots in SS20--"seats" are expensive
- The speed of some I/O devices is limited by human reaction time--very very slow by computer standard
- Examples: Keyboard and mouse
- No reason to use up one of the expensive SBus slot



Summary: Computer System Components



° **All have interfaces & organizations**